REMARKS

In the foregoing amendments, claim 1 was amended to define a semiconductor wafer having an outer peripheral face containing a notch having an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards a center of the semiconductor wafer. In addition, claim 1 defines that the notch contains markings made from dot marks respectively having a maximum length of 1 to 13 μm on the inner wall face. New claims 14 and 15 contain the limitations of claim 1. Claim 14 further defines that the semiconductor wafer comprises a marked semiconductor wafer made from a semiconductor wafer that was subjected to at least one additional fabrication step that is visibly discernible on the semiconductor wafer. Claim 15 further defines a semiconductor wafer having a peripheral surface that was treated with processing steps, so that the peripheral surface contains visibly discernible structure resulting from the processing steps; and the inner surface of the semiconductor wafer includes the notch, etc. Accordingly, claims 1-15 are in the application for consideration by the examiner.

In the foregoing amendments, claims 2 and 11 were amended as suggested in the objection to these claims that was set forth in section 2 on page 2 of the Official action. Therefore, applicant respectfully requests the examiner reconsider and withdraw the objection to the applicant's claims.

The Official action set forth two prior art rejections of the claims. The first was a rejection of claims 1 and 8-13 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,418,467 of Iwai in view of U.S. Patent No. 6,120,607 of Taravade (newly cited). This rejection is set forth on pages 3-5 of the Official action. Beginning near the bottom of page 5, claims 2-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwai and Taravade in further view of U.S. Patent No. 6,004,405 of Oishi *et al.* (Oishi).

Applicant respectfully submits that the teachings of Iwai, Taravade and/or Oishi either taken alone or in combination do not contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103.

Applicant respectfully submits that some of the positions taken in the outstanding Office action are simply an improper application of basic patent law. For example, the Official action stated that terms such as "inner," "outer," and "external" wall faces are merely relative terms, which do not patentably distinguish the claimed invention from Iwai in view of Taravade. However, applicant respectfully submits that terms such as "inner," "outer," and "external" are commonly used in patent law to distinguish over references. For example, there is a big difference between saying that the steering wheel of a vehicle is arranged on the *inner* side of the vehicle cab, or arranged on the *outer* side of the vehicle cab. The location of the notch with dot markings in the presently claimed semiconductor wafer distinguishes applicant's claimed

invention from the teachings cited thereagainst and, therefore, imparts patentability to applicant's claimed invention. The teachings cited against applicant's claims do not remotely contemplate or suggest a semiconductor wafer having an outer peripheral face having a notch with an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards a center of the semiconductor wafer, where the notch contains markings made from dot marks respectively having a maximum length of 1 to 13 μm on the inner wall face. The Official action does not explain where the teachings of the cited references contemplate or suggest this structure of the present claims.

Perhaps, the Office considers the presently claimed invention claimed to be simple. However, simplicity is not detrimental to patentability. See *Goodyear Tire & Rubber Co. v. Ray-O-Vac Co.*, 60 USPQ 386, 388 (1944) (simplicity of itself does not negative invention); *Panduit Corp. v. Dennison Mfg Co.*, 1 USPQ2d 1593, 1600 (Fed. Cir.) (the patent system is not foreclosed to those who make simple inventions), cert. denied, 481 U.S. 1052 (1987). Therefore, applicant respectfully submits that any alleged simplicity of the present claimed invention cannot bar it from patentability.

The Official action appeared to take the position that product-by-process phrases, such as "the markings being arranged on the inner surface of the notch prior to fabrication steps of a slicing step, and before a mirror faced fabrication step and chemical polishing step," and "upper and lower edge line

portions of the inner wall faced of the notch are respectively chamfered to thereby constitute upper and lower incline faces," do not lend patentability to applicant's claimed invention. Independent claim 1, as amended above, no longer contains such product-by-process phrases. New claim 14 defines that the semiconductor wafer comprises a marked semiconductor wafer made from a semiconductor wafer that was subjected to at least one additional fabrication step that is visibly discernible on the marked semiconductor wafer. New claim 15 defines a semiconductor wafer having a peripheral surface that was treated with processing steps, so that the peripheral surface contains visibly discernible structure resulting from the processing steps; and the inner surface of the semiconductor wafer includes the notch, etc. Both of these claims define a semiconductor wafer was subjected to at least one fabrication step that is *visibly discernible* on the surface of semiconductor wafer. For example, a semiconductor wafer that was polished has a surface that is *visibly discernible* from a semiconductor wafer that was not polished. Since the result of polishing (or other fabrication step) the semiconductor wafer is visibly discernible on the semiconductor wafer, a polished semiconductor wafer has a structure that is *visibly discernible* from an unpolished semiconductor wafer. Therefore, the expression such as "at least one fabrication step that is *visibly discernible* on the surface of semiconductor wafer" sets forth a structural limitation in the claim 14 and 15 that must be considered when determining the patentability of these claims. Similarly, the teachings of the cited

references must necessarily show or suggest inclined faces, as required in claims 2, 4, 5, 6, and 7.

Appellant respectfully submits that limitations in claims cannot be simply dismissed as denoting mere intended use and considered to have no limiting effect in comparing the claim with prior art reference, as alleged in the Official action. At best this appears to be an attempt to illicit a *per se* rule of claim construction and obvious, which the court explain in *Ochiai* are strictly prohibited. At worst this appears to be an attempt to circumvent basic patent principles laid down by the U.S. Supreme Court and the Court of Appeals for the Federal Circuit, which have repeatedly held that to ignore limitations in claims disregards several mainstay patent doctrines. See, e.g., *Continental Paper Bag Co. v. Eastern Paper Bag Co.*, 210 U.S. 405, 419 (1908) ("[T]he claims measure the invention."); *Pennwalt Corp. v. Durand-Wayland, Inc.*, 4 USPQ2d 1737 (Fed. Cir. 1987) (*in banc*), cert. denied, 485 U.S. 961, cert. denied, 485 U.S. 1009 (1988); *Perkin-Elmer Corp. v. Westinghouse Elec.*, 3 USPQ2d 1321 (Fed. Cir. 1987); *Lemelson v. United States*, 224 USPQ 526, 533 (Fed. Cir. 1985).

Perhaps, the most important difference between the teachings of the cited references and the presently claimed invention is the arrangement of the notch and, in more detail, where the markings are placed within the notch. Amended claim 1 and new claims 14 and 15 define that the notch extends inwardly and away from the outer peripheral face of the semiconductor and

towards a center of the semiconductor. Claim 14 also defines that the semiconductor wafer comprises a marked semiconductor wafer made from a semiconductor wafer that was subjected to at least one additional fabrication step that is visibly discernible on the marked semiconductor wafer. Claim 15 defines a semiconductor having a peripheral surface that was subjected to processing steps, so that the peripheral surface contains visibly discernible structure resulting from the processing steps; and the inner surface of the semiconductor wafer includes the notch, etc. Thus, both claims 14 and 15 define that a semiconductor that was subjected to a processing step and that resulted in structure that is visibly discernible on the semiconductor wafer. Those skilled in the art understand that the semiconductor wafer has a structure different before and after the processing step. For example, a polished semiconductor has a different structure than an unpolished semiconductor. Accordingly, these limitations in the applicant's claims must be considered when determining the patentability of the claims.

No teaching against the applicant's claims in the outstanding Office action remotely contemplates or suggests the notch as defined in claims 1, 14, and 15 and the combination of such a notch with markings thereon. During the semiconductor wafer-fabrication process, the semiconductor wafer receives various mechanical and chemical impacts. These fabrication steps include a chemical-mechanical polishing process. The location of the inner wall face of the notch, which extends inwardly and away from the outer peripheral face of

the semiconductor and towards a center of the semiconductor, as required in applicant's claims, is less likely to receive such mechanical and chemical impacts. Therefore, markings formed on the inner wall face of the notch, as required in applicant's claims, will survive during the fabrication process. For example, during fabrication, semiconductor wafers are conveyed by a robot, in which a robot's hands grasp the outer peripheral surface of the wafer. This causes mechanical impacts on the outer peripheral face of the semiconductor wafer. Applicant's claimed invention avoids the robot's hands destroying the dots marks, because the dots are marked on the notch, which is located in an area that will not be subjected to chemical and mechanical impacts. The teachings of the cited references do not contemplate or suggest arrangement of the notch and the markings thereon, as required in the present claims.

In addition, the outer peripheral surface of the semiconductor wafer, including its orientation flat face, is susceptible to be cracked. If markings are formed on our peripheral face, they are likely to be broken and disappear, during the processing of the semiconductor wafer. On the other hand, in the arrangement of the inter face wall the notch in accordance with applicant's claimed invention, which not extends inwardly towards the center of the wafer, the markings receive few, if any, mechanical impacts. Therefore, the markings in accordance with the presently claimed invention are not likely to disappear by cracking or otherwise.

The fabrication steps include chemical-mechanical polishing, where polishing is performed by flowing treatment liquid and applying an outer force on the outer peripheral face of the wafer including its orientation flat face. If markings appear on the outer peripheral face of the semiconductor wafer, such markings would most likely disappear during polishing. In other hand, in the presently claimed invention, although treatment liquid flows on the inner wall face of the notch; the inner wall face, which extends inwardly towards a center of the wafer, hardly receives any mechanical impact and, therefore, does not undergo mechanical polishing. For this reason, markings formed on the inner wall faced of the notch, as required in the present claims, are most likely to remain after the chemical-mechanical polishing step.

The teachings of Iwai propose a technology where markings are formed on the orientation flat face, which a different from the inner wall faced of the notch, which notch extends inwardly towards a center of the wafer, etc., as set forth in applicant's claims. In contrast to applicant's claims, the markings proposed by Iwai will most likely disappear from mechanical impacts and/or polishing steps, as discussed above.

The teachings of Yano propose forming marks on the chamfered face of the outer peripheral face of the wafer. However, these marks will most likely disappear from mechanical impacts and/or polishing steps, in contrast to applicant claims.

The teachings of Taravade merely propose the size of dots constituting the markings. These teachings do not contemplate or suggest the arrangement of a notch with markings as required in the present claims. Therefore, these teachings cannot cure or rectify the deficiencies in the teachings of Iwai and Yano, as discussed above.

For the foregoing reasons, applicant respectfully submits that none of the teachings of Iwai, Taravade, and Oishi, either taken alone or in combination, do not contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the prior art rejections of applicant's claims in the outstanding Office action.

In view of the foregoing amendments and remarks, favorable consideration and allowance of claims 1-15 are respectfully requested. While it is believed that all the claims in this application are in condition for allowance, should the examiner have any comments or questions, it is respectfully requested that the undersigned be telephoned at the below-listed number to resolve any outstanding issues.

In the event that this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge the fee therefor, as well as any deficiency in the payment of the required fee(s) or credit any overpayment, to our Deposit Account No. 22-0256.

Respectfully submitted,
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